OVERCOMING TOMBSTONES AND OPENS DUE TO THERMAL INEQUALITIES

Chris Schumacher
RiverSide Electronics, Ltd
Lewiston, MN
cschumacher@rellew.com

ABSTRACT

Tombstoning on small SMT chip packages are a common defect in electronic manufacturing. Multiple contributing factors can cause this phenomenon including varying thermal mass between opposing pads. The reflow profile can have a direct impact on tombstone occurrences. Two common industry profile techniques are used to compare the effects on tombstones with end of line defect data. Visual verification is done by duplicating test profiles on a rework station. The results show a clear benefit of one profile technique over another to reduce tombstoning.

INTRODUCTION

Tombstoning of small Surface Mount Technology (SMT) chip packages has been an ongoing defect since the introduction of surface mount components. Many factors contribute to this shortcoming. One of these factors may include board designs that do not have ideal pad layouts. This can be a problem in contract manufacturing if you are not included in the design or DFM process. Another factor is varying thermal mass between opposing pads. When focusing on thermal inequalities between pads, we investigate two common industry profile techniques to compare their effects on tombstones.

Cross-section image of problematic 0402. Image provided by **the Specialty Lab, Inc.**

HISTORY

SMT became popular in the 1980's, and it is now mainstream in the electronics industry. Since the introduction of SMT, tombstoning has remained a commonly encountered defect. Surface-Mount Technology for PC Board Design, James K. Hollomon, Jr. 1989 quotes a study done by a major paste manufacturer. "In a study of land size vs. tombstoning defects, *the paste manufacturer* found that the gap between the lands should essentially match the space between the terminations (bare body) on the component". At the time of this publication, 0805 was the smallest package size listed for their land pattern design recommendations. 40 years into SMT, we are still encountering tombstoning and searching for a resolution as package sizes continue to miniaturize.

THERMAL INEQUALITIES

Thermal inequalities develop during reflow from unequal masses between internal planes in the PCB. This can happen between lands of single component and result in one paste deposit turning liquidus before the other, promoting the opportunity for a tombstone or open. Figure 1a below shows an example of an open defect, Figure 1b highlights the thermal inequalities between pads.

Figure 1a: Open Defect

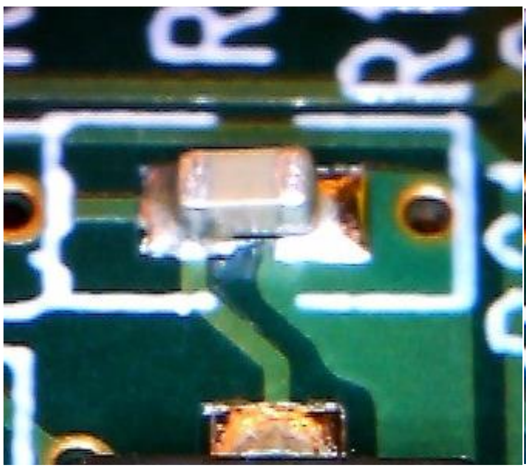
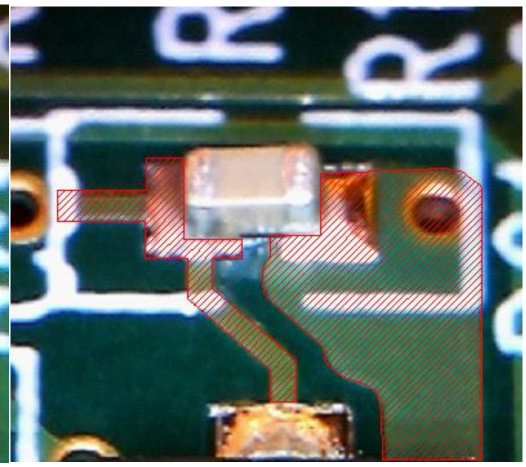


Figure 1b: Thermal Inequalities



The test vehicle is a multilayer PCB with Electroless Nickel Immersion Gold (ENIG) surface finish. This assembly was chosen for the test because of tombstoning and open defects, resulting in an unacceptable Defects per Million Opportunities (DPMO) on 0402 components.

Two thermal profiles were used to test their effects on tombstones. The two profiles being tested were the Ramp to peak (RP) which is the current profile and the Ramp to soak to Peak (RSP) which is the test profile. The RP (Figure 2) profile has a linear slope to its peak temperature. The RSP (Figure 3) profile has the addition of a soak, where the assembly is held at a very low ramp rate for a period of time in the middle of the profile which allows the assembly and components to reach a stable temperature.

As an initial test, and to visually compare the differences, the profiles were replicated on an offline rework station with a machine mounted camera allowing the reflow process to be recorded, documented and analyzed.

Final testing was completed using standard production practices on production units. This includes: screen printing, component pick and place, convection reflow and automated optical inspection (AOI). Results were analyzed using end of line data.

Figure 2: Example of a Ramp to Peak Profile (RP)

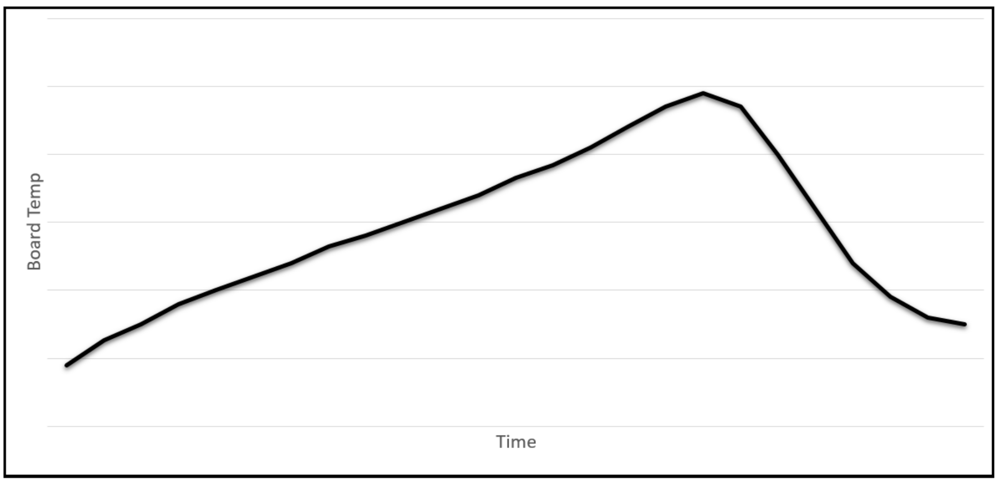
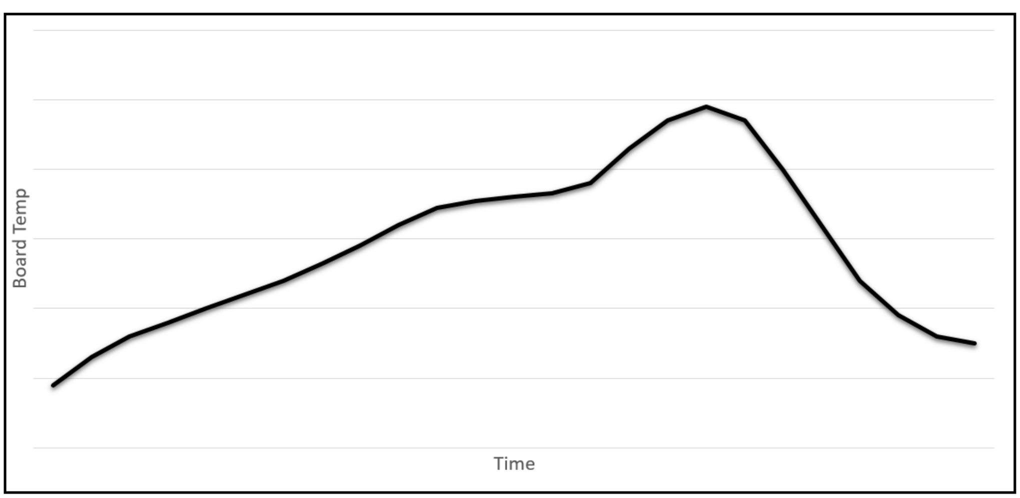


Figure 3: Example of a Ramp to Soak to Peak Profile (RSP)



INITIAL TESTING

To visually test unequal thermal qualities between pads the intended profile was replicated on a tabletop rework station. Figure 4 shows the RP profile with uneaqual thermal distrubition between the pads, with one solder deposit turning liquidus before the other which is likely a result of the higher ramp rate.

Figure 5 shows the RSP profile with an equal thermal distrubition between the pads, allowing the solder deposits on each pad to turn liquidus concurrently.

With initial testing showing promise for the RSP profile, it was determined the test was suitable for production testing.

Figure 4: Ramp to Peak (RP)

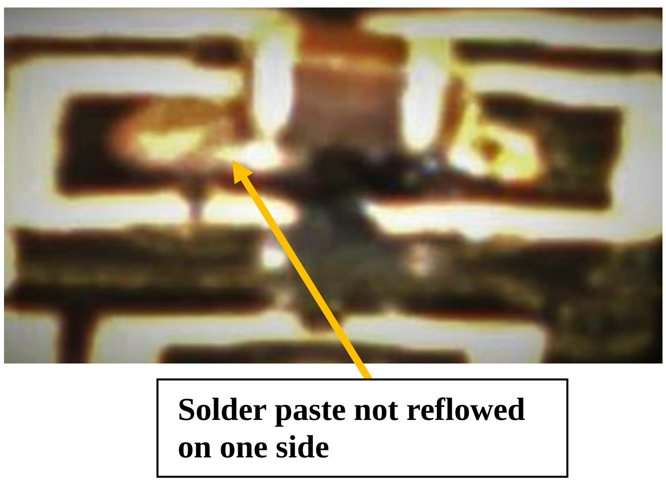
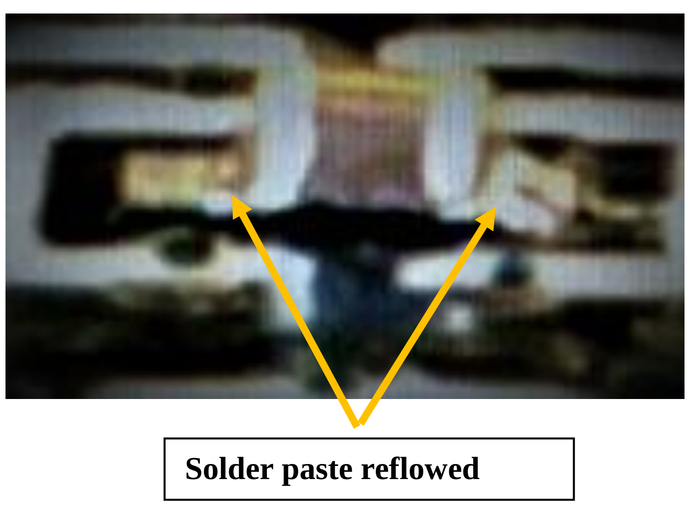
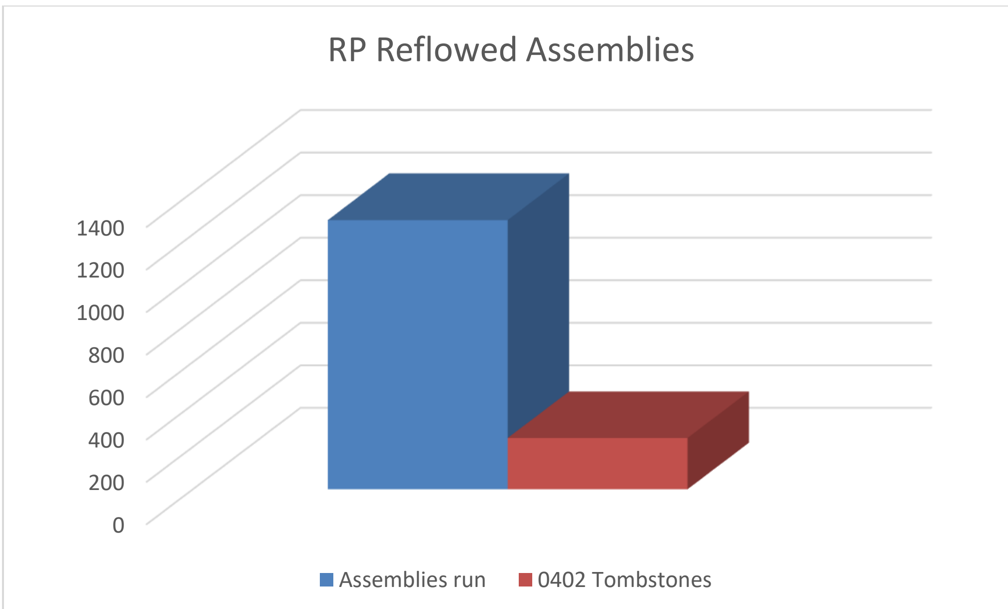


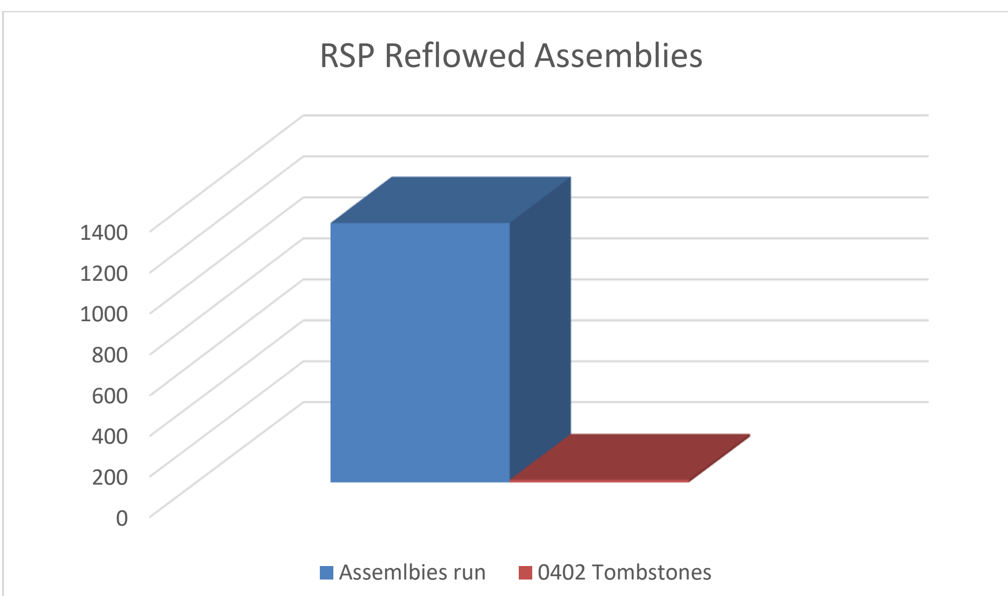
Figure 5: Ramp to Soak to Peak (RSP)



PRODUCTION TESTING

Between the testing of the RP and RSP profiles, over 2,400 assemblies and over 48,000 0402 components were used with each profile used approximatly 1200 boards and 24,000 0402 components. Results were a reduction of over 95% in tombstoning defects using the RSP profile vs using the RP profile.





CONCLUSION

With the multiple factors that contribute to tombstoning, the reflow profile continues to show an effect on tombstoning and opens. Equalizing thermal inequalities with the addition of a soak to the reflow profile has shown to reduce tombstones on 0402 components.

However, before making any thermal profile changes, be aware Thermal profiles tend to be product and paste specific. Before changing reflow profiles always contact your paste manufacturer and review component thermal limitations.

Laboratory analysis for this evaluation was provided by **The Specialty Lab, Inc.**

SOURCES

IPC-7530A: Guidelines for Temperature Profiling for Mass Soldering Processes-Reflow and Wave 2017

Surface-Mount Technology for PC Board Design, James K. Hollomon, Jr. 1989

The Specialty Lab, Inc. 1454 County Road C West, Roseville, MN 55113